## REMARKS

In the October 27, 2005 Office Action, the Examiner objected to the drawings, stating that the drawings should show the features of claims 5, 9 and 10. The Examiner also objected to claim 1 for an antecedent basis informality, rejected claims 1, 4-5, 7-8, 11 and 21 under 35 U.S.C. 102(b) as being anticipated by Publication No. 2002/0176288 to Nozuyama (hereinafter "Nozuyama") and Publication No. 2003/0023941 to Wang et al. (hereinafter "Wang"), and rejected claims 2-3, 6, and 9-10 under 35 U.S.C. 103(a) as being unpatentable over Nozuyama or Wang in view of Publication No. 2004/0015800 to Zhong et al. (hereinafter "Zhong"). Applicants respectfully traverse the objections and rejections for the reasons set forth hereinbelow.

### A. The Drawings Comply with 37 CFR § 1.83

In response to the Examiner's objection to the drawings, Applicants respectfully submit that Figure 2 illustrates claim 5's requirement of verifying the scan chain equivalency of first and second RTL models (two arrows from RTL description block 22) at the "formal verification" block 29. As for the "symbolic simulator" recitation of claims 9-10, Applicants submit that this feature is illustrated in at least Figure 2 (*e.g.*, "formal verification 29") and Figure 3 (*e.g.*, "processing block 33"). In view of the requirement in 37 CFR § 1.83 that the invention "should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (*e.g.*, a labeled rectangular box)" when a detailed illustration is not essential for a proper understanding of the invention, Applicants request that the Examiner reconsider and remove the objection to the drawings.

### B. Claim 1 Has Been Amended To Remove Antecedent Basis Objection

In response to the Examiner's objection to claim 1, Applicants have amended the claim to more clearly recite the antecedent basis. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objection to this claim.

### C. Claims 1, 4-5, 7-8, 11 and 21 Are Not Anticipated by Either Nozuyama or Wang

In response to the Examiner's rejection of claims 1, 4-5, 7-8, 11 and 21 as being anticipated by the Nozuyama and Wang references, Applicants respectfully request reconsideration and withdrawal of the rejection. As a preliminary matter, neither Nozuyama nor

Wang refers in any way to using symbolic expressions, and indeed, the term "symbolic" appears nowhere in either reference. More importantly, neither reference discloses or even remotely suggests how two different representations of a scan chain circuit design can be tested for equivalency. For example, Nozuyama discloses a testing process for a completed chip by reducing the length of the scan chain and reducing the number of observation points to simplify the test infrastructure. However, there is no mention made in Nozuyama of having two representations of a scan chain design that are compared for purposes of verifying equivalency therebetween. Likewise, Wang refers to an automated technique for creating and inserting scan chains in a design that does not already include a scan chain as an improvement over manual insertion of scan chains, but does not suggest any technique for comparing or verifying the equivalency of two different representations of a scan chain circuit design. Because neither Nozuyama nor Wang discloses how two different representations of a scan chain circuit design are to be compared for scan chain equivalency using symbolic expressions, Applicants respectfully request that the anticipation rejections of claims 1, 4-5, 7-8, 11 and 21 be withdrawn and that the claims be allowed.

**D. Claims 2-3, 6, and 9-10 Are Not Obvious Over Nozuyama or Wang in view of Zhong**

Applicants respectfully submit that the deficiencies of the Nozuyama and Wang references outlined above are not remedied by the disclosure of Zhong. While Zhong discloses performing a symbolic simulation of a functional design, there is no mention in Zhong of verifying the scan chain equivalency between two different scan chain circuit designs. Indeed, Applicants expressly distinguished Zhong in the application with the statement that:

> While symbolic simulation has been used in connection with functional design verification applications (such as described in U.S. Patent No. 6,634,012 to Zhong et al., which is hereby incorporated by reference in its entirety), the present invention contemplates a new and hitherto undisclosed application of symbolic simulation to perform scan chain equivalency verification. In a selected embodiment, equivalency checking of scan chain test structures in memory designs is performed using symbolic simulation of the differing test structure circuit models....

Application, p. 8 (paragraph 23). Accordingly, Applicants respectfully request that the obviousness rejection of claims 2-3, 6, and 9-10 be withdrawn and the claims be allowed.

## CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and Applicants respectfully request that the Examiner withdraw the drawing objections, the objection to claim 1 and the rejection of the pending claims over the prior art, and that a Notice of Allowance be issued. If there are any remaining issues that might be resolved through a telephonic interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

I hereby certify that this correspondence is being transmitted via facsimile to the USPTO on December 19, 2005.

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Respectfully submitted,

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